1. (Amended) A multi-layered semiconductor device characterized in that a film-like semiconductor package incorporating therein a semiconductor chip is disposed in a package accommodation opening of a circuit pattern layer to form a circuit board, said circuit pattern layer comprises a substrate, a circuit pattern formed on the substrate, and said package accommodation opening, and a plurality of such circuit boards are layered together to electrically connect said circuit patterns of the respective circuit boards with each other.

REMARKS

Claims 1-18 are pending in this application. Claims 6-10, 17 and 18 are withdrawn from consideration. Claims 1-5 and 11-16 are rejected. Claim 1 has been amended to more particularly point out and distinctly claim Applicants' invention. No new matter is added. The features present in the claims as amended were present in the originally filed specification.

The Invention as set forth in Claims 1-5

The present invention as set forth in amended Claim 1 is directed to a multi-layered semiconductor device which has a film-like semiconductor package which incorporates a semiconductor chip. The film-like semiconductor package is disposed in a package accommodation opening of a circuit pattern layer. The film-like semiconductor package having the semiconductor chip incorporated therein and the circuit pattern layer together form a circuit board. In the invention as claimed in Claim 1, each circuit pattern layer comprises a substrate, a circuit pattern formed on the substrate and the package accommodation opening. A plurality of the circuit boards formed from the film-like

semiconductor package and the circuit pattern layer are layered together to electrically connect the circuit patterns of the respective circuit boards with each other.

According to the present invention, as set forth in Claims 1-5, a multi-layered semiconductor device is produced which has a number of semiconductor chips. The resulting semiconductor device can also have a relatively complicated wiring or circuit structure. For example, a micro-chip module (MCM) can be obtained according to the present invention. As a result of the present invention, greater efficiencies and yields can be obtained as compared to previous semiconductor devices.

One advantage that the present invention offers is that one can test or individually check the chips before they are incorporated into the semiconductor package thereby saving the time, effort and expense which occurs in the event that a particular semiconductor chip is found to be defective.

The Rejection of Claims 1-5 under 35 U.S.C. 103(a)

The Examiner has rejected Claims 1-5 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto. Applicants hereby traverse the rejection of the Claims.

In paragraph 1 of page 2 of the Office Action, the Examiner rejected Claims 1-5 under 35 U.S.C. 103(a) as being unpatentable over Miyamoto. The reference fails to teach at least a circuit pattern on the device and the cited reference does not provide any suggestion, motivation or teaching for providing one and arriving at the present invention.

The Office Action states that Miyamoto discloses a multi-layered semiconductor device wherein a semiconductor package incorporates a semiconductor chip to form a circuit board. The Office Action then states that a plurality of such circuit boards are layered together to electrically connect circuit patterns of the respective circuit boards with each other. At the top of page 3 of the Office Action, the Examiner admits that Miyamoto

does not disclose a circuit pattern layer but then states that the teaching of etching the copper foil to form leads and holes obviously means that a circuit pattern is formed.

It is respectfully submitted that the invention of Miyamoto is directed to an altogether different structure than that of Applicants. The cited portions of Miyamoto, and more particularly Fig. 34, are directed to a structure having a chip AD having leads 5b on one side of the chip. A tape carrier 2b is on leads 5b. Adhesive 10 adheres the bottom of the leads 5b to the top of top tape carrier 2a. In addition, another chip MF has leads 5a which extend underneath bottom tape carrier 2a.

It is respectfully submitted that the above-described device structure does not include a circuit pattern layer nor is it obvious to provide a circuit pattern such as Applicants' as suggested by the Examiner such that one of ordinary skill in the art would arrive at applicant's invention.

Applicant offers the following arguments in support of their arguments traversing the rejection by means of reference to Figures 2a and 2b in the present application. Applicants' reference to the circuit board which is one of a plurality of circuit boards in one embodiment of the claimed invention as set forth in the aforementioned Figures is by way of example only, and is not intended to limit the scope of the claims.

As set forth beginning on page 9, line 33, Applicants' invention as seen in Figures 2a and 2b is directed to a semiconductor package 10 having a chip 12 accommodated in an opening 11c shown in Fig. 2b. The semiconductor device has a circuit pattern layer which is comprised of a circuit pattern 13 and substrate 11. As set forth in the Claim 1 the film-like semiconductor package and the circuit pattern layer form one of a plurality of circuit boards, said circuit boards being layered together to electrically connect the circuit patterns of the respective circuit boards with each other.

Based on the foregoing, Applicants submit that one of ordinary skill in the art would not arrive at the present invention by modifying the Miyamoto reference by providing a circuit pattern layer on the device shown in Fig. 34. Even if one were to modify the structure disclosed in the reference as suggested by the Examiner, the resulting device would not be the claimed invention due to the aforementioned structural differences between the claimed semiconductor device and the device of Miyamoto. The Miyamoto reference simply fails to teach a circuit pattern layer comprising a substrate, a circuit pattern formed on the substrate and a package accommodation opening.

Applicants respectfully submit the rejection of Claims 1-5 over Miyamoto should be withdrawn.

The Rejection of Claims 11-13, 15 and 16

The Examiner has rejected Claims 11-13, 15 and 16 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto. Applicants hereby traverse the rejection of the Claims.

It is respectfully submitted that the portions of the Miyamoto reference cited by the Examiner do not teach nor render obvious the invention of independent Claim 11 and the claims which depend therefrom. Claim 11 has the features of a plurality of circuit boards layered together wherein each circuit board comprises an insulation substrate, a semiconductor chip incorporated in the substrate and a circuit formed on a surface of the substrate and connected to the semiconductor chip. In addition, a lead extends from the circuit on the circuit board and is bonded to another circuit board disposed beneath the first circuit board to establish an interlayer connection by way of the lead going through a through-hole provided in the insulation substrate.

As stated above, Miyamoto fails to teach a circuit on a surface of a substrate having a semiconductor device nor does Miyamoto provide any suggestion, motivation or teaching for the same. Accordingly, it requested that the 35 U.S.C. 103(a) rejection must be withdrawn. Fig. 27

The Rejection of Claim 14 under 35 U.S.C. 103(a)

The Examiner has rejected Claim 14 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto in view of Smith, U.S. Patent Application Publication No. U.S.2001/0001989. Applicants hereby traverse the rejection of the Claim.

It is respectfully submitted that the proffered combination of references cannot render the rejected claims obvious because the secondary Smith reference does not provide the teaching noted above with respect to the above-described features which are absent from the primary Miyamoto reference. Smith only discloses a beam lead for electrically connecting a chip to a circuit board. However, there is no suggestion in Smith that a lead is extended from the circuit to electrically connect with a circuit board through a through-hole. Thus, the combination of the cited references fails to teach or suggest all the claim limitations.

Based on the reasoning stated above, Applicant believes one of ordinary skill in the art would not arrive at the present invention by combining Miyamoto with Smith. Therefore, reconsideration of the rejection of Claim 14 and its allowance is respectfully requested.

CONCLUSION

For the reasons set forth above, Applicants' present invention, as recited in the amended claims now more clearly and particularly, is patentable. Reconsideration and

withdrawal of all outstanding rejections and objections in this case is hereby respectfully requested.

If further matters remain in connection with this case, the Examiner is invited to telephone the Applicant's undersigned representative to resolve them.

Respectfully submitted,

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Order No. 1041

Marked copy of the claims pursuant to 37 C.F.R. Section 1.121(c)

1. (Amended) A multi-layered semiconductor device characterized in that a film-like semiconductor package incorporating therein a semiconductor chip is disposed in a package accommodation opening of a circuit pattern layer to form a circuit board, said circuit pattern layer comprises a substrate, a circuit pattern formed on the substrate, and said package accommodation opening, and a plurality of such circuit boards are layered together to electrically connect said circuit patterns of the respective circuit boards with each other.